REMARKS

Claims 1, 2 and 23-26 are rejected; and claims 3-10 are allowed.

Review and reconsideration on the merits are requested.

Claims 1 and 2 have been canceled. Claims 3 and 4 have been amended to delete the limitation "the plurality of electrically conductive vias all having a straight shape." Claims 23-25 have been amended to recite that the capacitor main body has an uppermost ceramic surface 92 on which a semiconductor device 21 having surface-connecting terminals is to be mounted.

Entry of the amendments at this stage is respectfully requested as placing the case in condition for allowance.

Claims 23-26 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,775,150 to Chakravorty et al. Chakravorty et al. was cited as disclosing the claimed capacitor, including a plate-shaped capacitor (141 & 151) main body having a first ceramic surface on which a semiconductor device (60) having surface-connected terminals is to be mounted.

Applicants respectfully traverse for the following reasons.

Fig. 3 of Chakravorty et al. cited by the Examiner illustrates a cross-section of the die/substrate structure of Fig. 2, where the multilayer substrate comprises an organic portion 80 and a ceramic portion 90. Organic portion 80 comprises a plurality of organic layers 81-83, and is provided for routing and fanning out of conductor traces for I/O signals (column 4, lines 49-52). Thus, contrary to the Examiner's suggestion, Chakravorty et al. does not disclose an approximately plate-shaped capacitor main body having a first ceramic surface on which a

semiconductor device having surface-connecting terminals is to be mounted as required by the rejected claims. Rather, the assembly of Chakravorty et al. has a corresponding first organic surface on which a semiconductor device is to be mounted.

To more clearly distinguish over Chakravorty et al., claims 23-26 have been amended to recite that the capacitor main body has an uppermost ceramic surface on which a semiconductor device having surface-connecting terminals is to be mounted.

Withdrawal of the foregoing rejection under 35 U.S.C. § 103(a) is respectfully requested.

In response to the rejection of claims 1 and 2 under 35 U.S.C. § 103(a) as being unpatentable over Chakravorty et al. in view of U.S. Patent No. 6,072,690 to Farooq et al., claims 1 and 2 have been canceled.

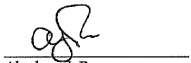
The Examiner considered the patentable feature of claim 3 to reside in the limitation "wherein the thermal expansion coefficient of the capacitor main body is smaller than that of the substrate." Accordingly, the limitation "the plurality of electrically conductive vias all having a straight shape" is not needed to distinguish over the prior art and claims 3 and 4 have been amended to delete the subject limitation.

Withdrawal of all rejections and allowance of claims 3-10 and 23-26 is earnestly solicited.

In the event that the Examiner believes that it may be helpful to advance the prosecution of this application, the Examiner is invited to contact the undersigned at the local Washington, D.C. telephone number indicated below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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Date: April 26, 2007